SECAM chroma signal processor for VHS VCRs

BA7107/BA7107F/BA7107S

The BA7107, BA7107F and BA7107S are monolithic ICs that incorporate the principle circuits required for SECAM chroma signal processing. The ICs are divided into recording system and playback system blocks.
The recording system consists of a REC EQ amplifier, a divide–by–four circuit, a limiter amplifier, an anti–bell amplifier, and a REC sync gate, and the playback system consists of PB EQ amplifier, a multiply–by–four circuit (two multiply–by–two circuits), a limiter amplifier, a bell amplifier, and a PB sync gate. Switching between the recording and playback systems is accomplished by switching power supplies.

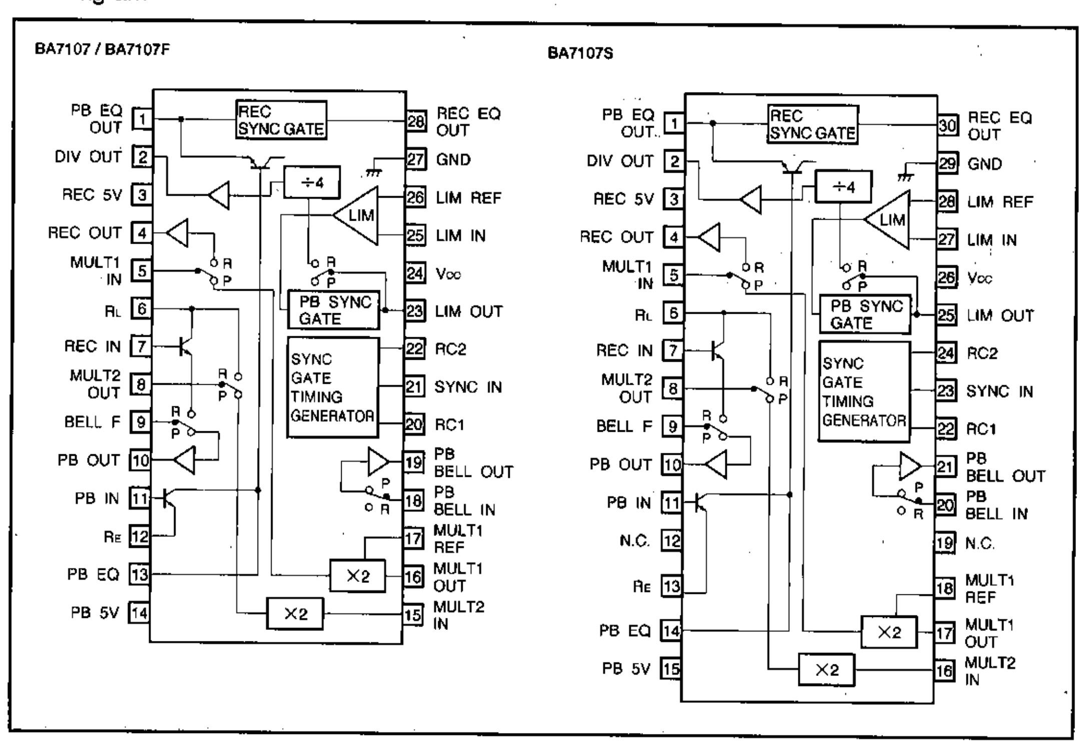
●Applications

SECAM and VHS format video cassette recorders

●Features

1)Recording and playback processor for SECAM chroma signals can be constructed using a single IC.
2)Switching between the recording and playback systems is accomplished by switching power supplies.
3)Operates off a 5V power supply voltage and is suitable for use in low voltage portable sets.
4)Available in SOP, DIP and SDIP packages (BA7107F: SOP28, BA7107: DIP28 and BA7107S: SDIP30).

●Block diagram



ROHM

●Absolute maximum ratings (Ta=25℃)

Parameter		Symbol	Limits	Unit
Power supply voltage		Vcc	6.5	V
Power dissipation	BA7107	Pd	1000 *	mW
	BA7107F / S		600 *	
Operating temperature		Topr	−10~65	℃
Storage temperature		Tstg	−55~125	℃

* Reduced by 10mW (BA7107) and 6mW (BA7107F/S) for each increase in Ta of 1°C over 25°C.

●Electrical characteristics (Unless otherwise specified : Ta=25℃, Vcc=5V, REC system: REC5V=5V, PB system: PB5V=5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply voltage	V_{CC}	4.5	5	5.5	V	Common power supply and same voltage for REC and PB
Limiter amplifier output level (pin 23)	V_{OLIM}	0.75	1.10	1.45	V	f_{IN}=4.3MHz, V_{IN}=10mV (25pin)
Limiter amplifier gain (pin 23)	G_{VLIM}	38	52	62	dB	f_{IN}=4.3MHz, V_{IN}=0.5mV (25pin)
F/F output level (pin 2)	$V_{O(F/F)}$	0.35	0.50	0.65	V_{P-P}	f_{IN}=4.3MHz, V_{IN}=10mV (25pin)
REC gate isolation (pin 1)	I_{SOR}	−25	−40	−	dB	f_{IN}=1MHz, V_{IN}=0.5V_{P-P} (28pin)
PB gate isolation (pin 23)	I_{SOP}	−20	−30	−	dB	f_{IN}=4.3MHz, V_{IN}=0.5mV (25pin)
2-stage multiplier output level (pin 16)	$V_{O(X2)}$	0.25	0.4	0.55	V_{P-P}	f_{IN}=1MHz, V_{IN}=0.2V_{P-P} (5pin)
1st harmonic distortion (pin 16)	$D_{1(X2)}$	−	−30	−20	dB	f_{IN}=1MHz, V_{IN}=0.2V_{P-P} (5pin)
3rd harmonic distortion (pin 16)	$D_{2(X2)}$	−	−35	−20	dB	f_{IN}=1MHz, V_{IN}=0.2V_{P-P} (5pin)
4-stage multiplier output level (pin 8)	$V_{O(X4)}$	0.09	0.14	0.25	V_{P-P}	f_{IN}=2MHz, V_{IN}=0.3V_{P-P} (15pin)
1st harmonic distortion (pin 8)	$D_{1(X4)}$	−	−30	−20	dB	f_{IN}=2MHZ, V_{IN}=0.3V_{P-P} (15pin)
3rd harmonic distortion (pin 8)	$D_{2(X4)}$	−	−35	−20	dB	f_{IN}=2MHz, V_{IN}=0.3V_{P-P} (15pin)
Quiescent current (PB mode)	$I_{Q(PB)}$	−	38	52	mA	−
Quiescent current (REC mode)	$I_{Q(REC)}$	−	40	52	mA	−
REC gate amplifier gain (pin 1)	G_{VRG}	7.5	9.5	11.5	dB	f_{IN}=1MHz, V_{IN}=70mV (28pin)
SYNC threshold voltage (pin 21)	V_{TH}	1.0	1.35	2.0	V	Voltage at which SYNC gate operates.
Chroma killer level	V_{CK}	−	4.7	4.9	V	f_{IN}=1.1MHz, V_{IN}=0.2V_{P-P} (5pin)
Pin 20 timing (pin 20)	T_1	48	56	64	μs	R_T=100kΩ, C_T=1000pF, SYNC IN : 21pin
Pin 22 timing (pin 22)	T_2	4.4	5.2	6.0	μs	R_T=120kΩ, C_T=33pF, SYNC IN : 21pin
Gate output offset (pin 1, pin 23)	V_{OSG}	−0.1	−	0.1	V	V_{IN} = 0V for both REC and PB

* Pin numbers are for the DIP (BA7107) and SOP (BA7107F) packages.

●Measurement circuits

BA7107/BA7107F

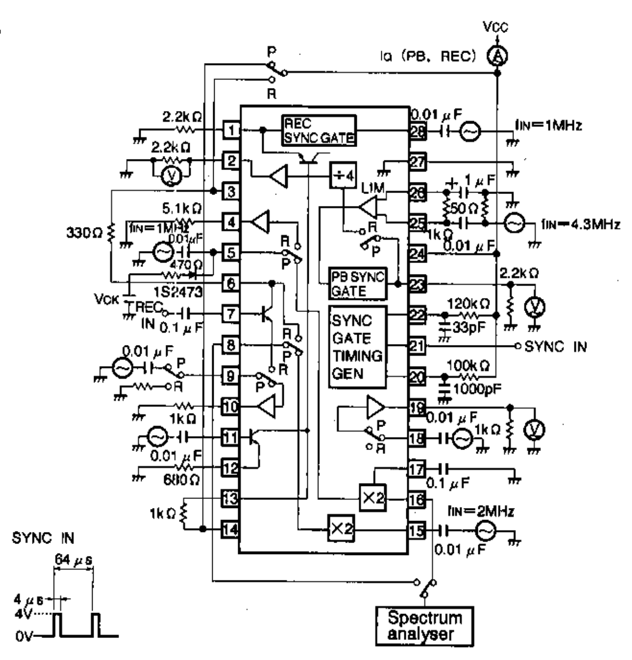


Fig.1

●Application example

BA7107/BA7107F

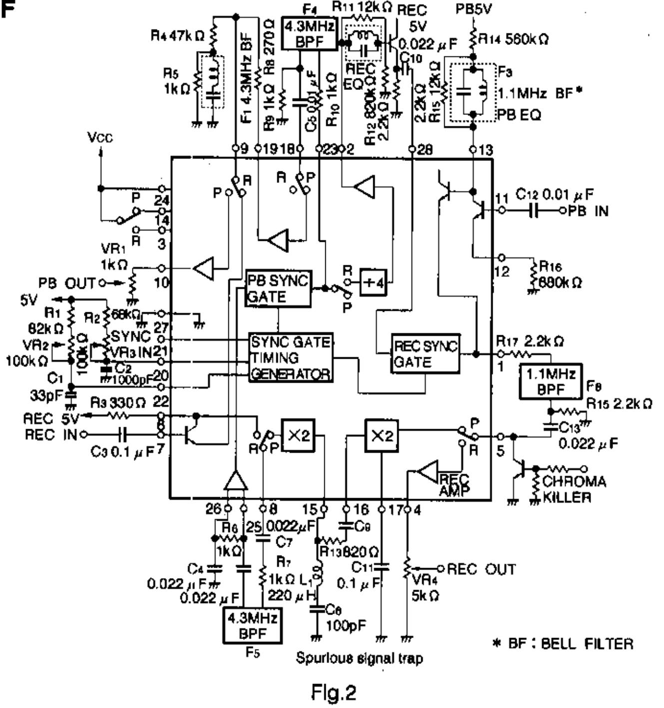


Fig.2

●Recording/playback mode signal flow

BA7107/BA7107F

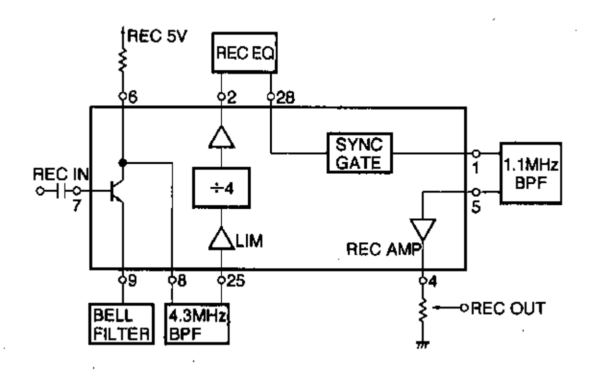
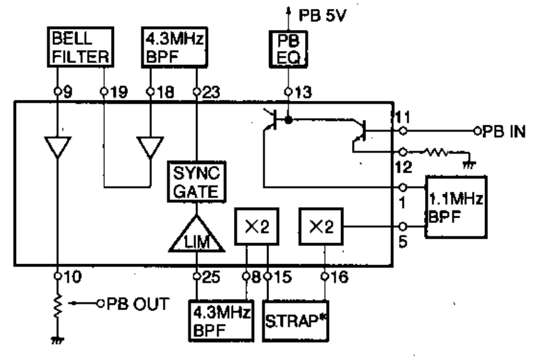


Fig. 3 Recording mode

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* S.TRAP : Spurious signal trap

Fig. 4 Playback mode

●SYNC gate timing

BA7107/BA7107F

The SYNC gate opens T_2 seconds after the rising edge of the SYNC IN signal from pin 21, and closes T_1 seconds after the falling edge of the signal (see Fig. 5). T_1 is set by the time constant of the CR circuit connected to pin 20, and T_2 by the time constant of the CR circuit connected to pin 22.

The REC and PB SYNC gates are closed for an interval determined by T_1 and T_2 during horizontal scanning (SYNC IN: 64 μS), and the gates stay closed during vertical retrace (the SYNC IN input pulse period becomes shorter than T_1; 32 μS). Refer to Fig. 6.

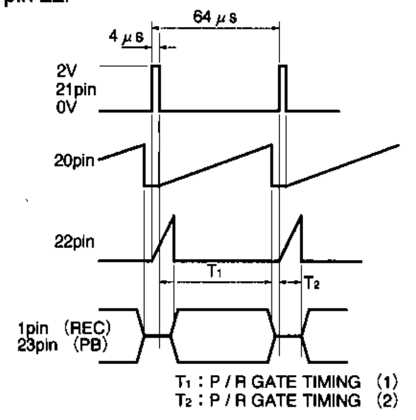


Fig. 5 P/R gate timing chart

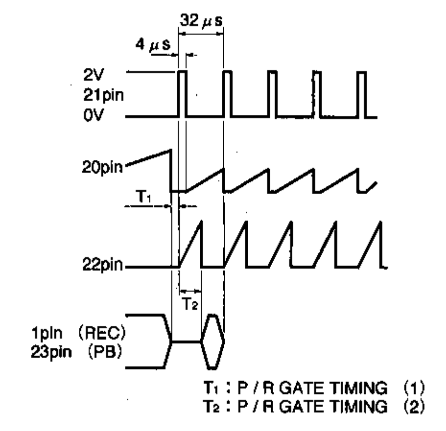


Fig. 6 P/R gate timing chart (V interval)

●Recording/playback switching

Switching between recording and playback is accomplished by switching power supply terminals. The IC is in recording mode when power is supplied to the Vcc pin (pin 24) and the REC5V pin (pin 3), and is in playback mode when power is supplied to the Vcc pin (pin 24) and the PB5V pin (pin 14).

Mode	Vcc (24pin)	REC 5V(3pin)	PB 5V(14pin)
REC	ON	ON	OFF
PB	ON	OFF	ON

* The pin numbers given above are for the DIP and SOP packages.

●Electrical characteristic curves

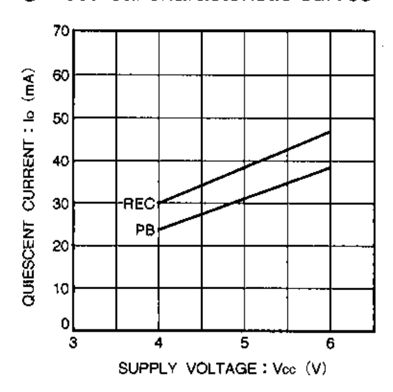


Fig. 7 Quiescent current vs. supply voltage characteristic

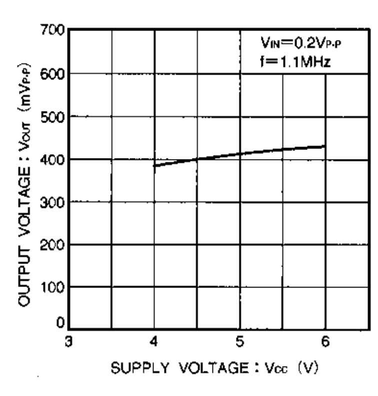


Fig. 8 2-stage multiplier circuit output level vs.supply voltage characteristic

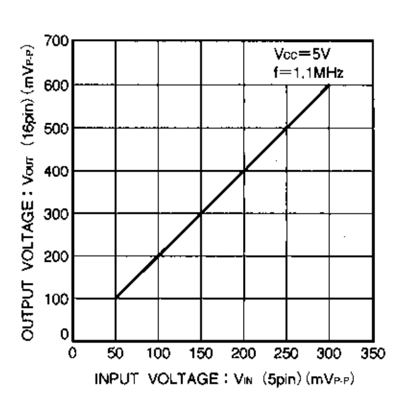


Fig. 9 2-stage multiplier circuit input voltage vs. output voltage characteristic

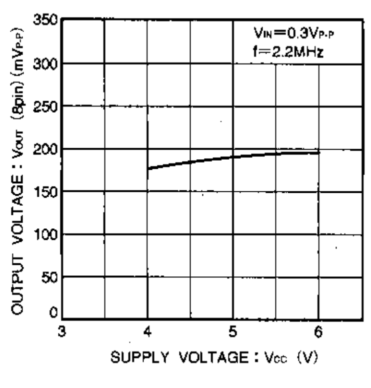


Fig. 10 4-stage multiplier circuit output voltage vs. supply voltage characteristic

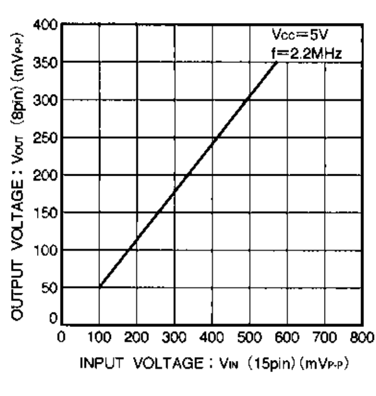


Fig. 11 4-stage multiplier circuit input voltage vs. input voltage characteristic

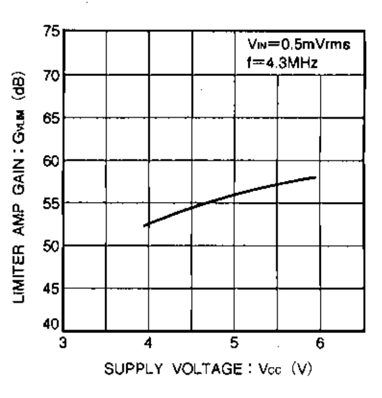


Fig. 12 Limiter amplifier gain vs. supply voltage characteristic

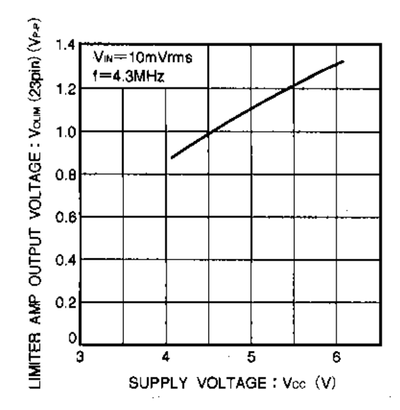


Fig. 13 Limiter amplifier output voltage vs. supply voltage characteristic

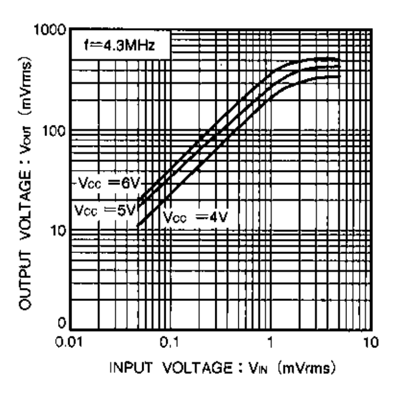


Fig. 14 Limiter amplifier gain vs. input voltage characteristic

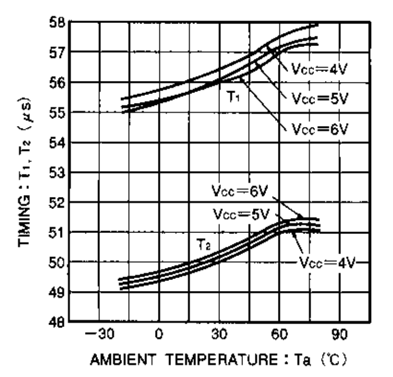


Fig. 15 One-shot timing period vs. ambient temperature characteristic

●External dimensions (Units: mm)

